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Confirmation No. 3565

Patent

C. Davis

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In re Application of:

John F. McMahon

Serial No.: 09/768,580

Filed: January 23, 2001

For: METHOD OF FABRICATING A STACKED CHIP PACKAGE

Examiner: Chambliss, A.

Art Unit: 2827

Box RCE
Commissioner for Patents
Washington, D.C. 20231

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

In response to the Final Office Action mailed April 3, 2002, Applicant respectfully requests continued examination (RCE) per 37 CFR 1.114 and for the Examiner to enter the following amendments and to consider the following remarks.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Box RCE, Commissioner for Patents, Washington, D. C. 20231

on October 1, 2002
(Date of Deposit)

Dianne Neathery
(Typed or printed name of person mailing correspondence)

Dianne Neathery
Signature

10/1/02
Date

IN THE CLAIMS:

Claims 21-27 are pending. Claims 21-27 are rejected. Applicant has included all pending claims for the Examiner's convenience. Please replace claim 21 with the following claim 21:

C1

21. (twice amended) A method of constructing a multi-chip package, comprising:

placing a first chip package on a first shelf;

electrically attaching said first chip package to a plurality of shelves with direct connections between said first chip package and said plurality of shelves;

placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and

electrically attaching said second chip package to said second shelf with direct connections between said second chip package and said second shelf.

22. (amended) The method of claim 21 further comprising the step of filling said multi-chip package above said second chip package with an encapsulant.

23. (amended) The method of claim 22 wherein said step of placing said second chip package on said second shelf further comprises placing said second chip package on said second shelf with a sealer such that a sealed open cavity below said second shelf protects said first chip package.

24. (amended) The method of claim 21 wherein said step of placing said first chip package further comprises placing a CPU chip package on said first shelf.

25. (amended) The method of claim 21 wherein said step of placing said second chip package further comprises placing a memory cache on said second shelf.

26. (amended) The method of claim 21 wherein said step of electrically attaching said first chip package further comprises wire bonding said first chip package to said plurality of shelves.

27. (amended) The method of claim 21 wherein said step of electrically attaching said second chip package further comprises wire bonding said second chip package to said plurality of shelves.

IN THE SPECIFICATION

Please replace the first full paragraph on page 11 beginning on line 9 of the specification with the following paragraph:

C2

Once the CPU die 26 and its supporting slug 24 have been attached to the ceramic package 17, the CPU die 26 is electrically connected to the package 17 via wire bonds I 28 and 30 (step 52). Note the fabrication of a standard ceramic PGA package having a CPU device bonded to a plurality of shelves would end here. The partially fabricated chip package 10 could easily be tested for functionality at this point. However, testing at this point is purely optional.

STATUS OF CLAIMS

The Examiner has rejected claims 21 - 27.

REMARKS

37 CFR §1.84(p)(5) drawing objections

The Examiner has objected to the drawings as failing to comply with 37 CFR §1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 52. Correction is required.

Applicants have amended the specification to incorporate the 52 (i.e. step 52) reference in FIG. 2.

35 USC §102(b) rejections

The Examiner has rejected claims 21, 26, and 27 under 35 USC §102(b) as being anticipated by Kiyoski (JP 4-219966)

The Examiner states that with respect to Claim 21, *Kiyoski* places a first chip package 4 on a first shelf, which is electrically attached to a plurality of shelves that are electrically attached to pin 1 (see Fig. 1). Pin 1 electrically attaches the multi-chip package to an external device, which means that the plurality of shelves are in electrical communication with each other by way of pins 1 resulting in the first chip package 4 being also in electrical communication with the plurality of shelves. A second chip package 4 (i.e. the chip above the first chip package) is electrically attached to the second shelf (see English abstract and figures).

Applicant claims in amended claim 21, "A method of constructing a multi-chip package, comprising: placing a first chip package on a first shelf; electrically attaching said first chip package to a plurality of shelves with direct connections between said first chip package and said plurality of shelves; placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and electrically attaching said second chip package to said second shelf with direct connections between said second chip package and said second shelf." As such, Applicant claims a first chip package that is attached to a plurality of shelves by a direct connection between the first chip package and the plurality of shelves. The Examiner has argued that the *Kiyoshi* reference discloses, as a result of all electrical connections such as the pins, a chip in electrical communication with the plurality of shelves. Applicant's amended claim 21 for attaching the chip and the plurality of shelves with a direct connection is distinct from *Kiyoshi,* which discloses an electrical connection that may be possible somewhere in the overall circuitry.

With respect to claims 26 and 27, Applicant argues that these claims depend on independent claim 21 and as such should be allowed for at least the same reasons as claim 21 is patentable.

Claims 21, 26, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu (U.S. 5,633,530).

The Examiner argues that with respect to claim 21, Hsu places a first chip package 13a on a first shelf, which is electrically attached to the plurality of shelves, since the plurality of shelves are electrically attached to pin 20. Pin 20 electrically attaches the multi-chip package to an external device, which means that the plurality of shelves are in electrical communication with each other by way of pins 20 resulting in the first chip package 13a being also in electrical communication with the plurality of shelves. A second chip package 13b is electrically attached to the second shelf (see Fig. 1).

Applicant claims in amended claim 21, "A method of constructing a multi-chip package, comprising: placing a first chip package on a first shelf; electrically attaching said first chip package to a plurality of shelves with direct connections between said first chip package and said plurality of shelves; placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and electrically attaching said second chip package to said second shelf with direct connections between said second chip package and said second shelf." As such, Applicant claims a first chip package that is attached to a plurality of shelves by a direct connection between the first chip package and the plurality of shelves. The Examiner has argued that the *Hsu* reference discloses, as a result of all electrical connections such as wire bonds, a chip in electrical communication with the plurality of shelves. Applicant's amended claim 21 for attaching the chip and the plurality of shelves with a direct connection is distinct from *Hsu,* which discloses an electrical connection that may be possible somewhere in the overall circuitry.

With respect to claims 26 and 27, Applicant argues that these claims depend on amended independent claim 21 and as such should be allowed for at least the same reasons as claim 21 is patentable.

<u>35 USC §103(a) rejections</u>

Examiner rejected claims 22 and 23 under 35 U.S.C.103(a) as being unpatentable over <u>Hsu</u> (U.S. 5,633,530) as applied to claim 21 above, and further in view of <u>Chia et al</u>. (U.S. 5,563,446).

With respect to claims 22 and 23, Applicant argues that these claims depend on amended independent claim 21 and as such should be allowed for at least the same reasons as claim 21 is patentable.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 5,633,530) as applied to claim 21 above, and further in view of Wenzel et al. (U.S. 6,150,724).

With respect to claims 24 and 25, Applicant argues that these claims depend on amended independent claim 21 and as such should be allowed for at least the same reasons as claim 21 is patentable.

It is respectfully submitted, that in view of the amended application title, amended specification paragraphs, amended claims, and the remarks set forth herein, all requests by the Examiner have been met and all rejections and objections overcome.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such an extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: October 1, 2002

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